SELF-TEST ARCHITECTURE TO IMPLEMENT DATA
COLUMN REDUNDANCY IN A RAM

ABSTRACT OF THE DISCLOSURE

Self-test architectures are provided to implement data column and row redundancy with a totally integrated self-test and repair capability in a Random Access Memory (RAM), either a Dynamic RAM (DRAM) or a Static Ram (SRAM), and are particularly applicable to compileable memories and to embedded RAM within microprocessor or logic chips. The invention uses two passes of self-test of a memory. The first pass of self-test determines the worst failing column, the column with the largest number of unique failing row addresses. After completion of the first pass of self-test, the spare column is allocated to replace the worst failing column. In the second pass of self-test, the BIST (Built In Self-Test) collects unique failing row addresses as it does today for memories with spare rows only. At the completion of the second pass of self-test, the spare rows are then allocated. Once the second pass of self-test is completed, the column and unique failing row addresses are transported to the e-fuse macros and permanently stored in the chip.